

	L #	Hits	Search Text	DBs
1	L1	4180	(sequenc\$3 issu\$3 dispatch\$3) near10 instruction near20 ((composite comput\$5 process\$3 operation\$3 function\$3) adj2 (block unit module engine subunit element subsystem))	USPAT; US-PGPUB
2	L2	455796	(status state condition) near10 (network rout\$3 bus connect\$3 interconnect\$3 path line)	USPAT; US-PGPUB
3	L3	7078	2 near20 ((composite comput\$5 process\$3 operation\$3 function\$3) adj2 (block unit module engine subunit element subsystem))	USPAT; US-PGPUB
4	L4	522	1 and 3	USPAT; US-PGPUB
5	L5	35351	((composite comput\$5 process\$3 operation\$3 function\$3) adj2 (block unit module engine subunit element subsystem)).ab,ti.	USPAT; US-PGPUB
6	L7	594	(sequenc\$3 issu\$3 dispatch\$3) near10 instruction near20 ((composite comput\$5 process\$3 operation\$3 function\$3) adj2 (block unit module engine subunit element subsystem))	EPO; JPO; DERWENT; IBM_TDB
7	L8	277642	(status state condition) near10 (network rout\$3 bus connect\$3 interconnect\$3 path line)	EPO; JPO; DERWENT; IBM_TDB
8	L9	2470	8 near20 ((composite comput\$5 process\$3 operation\$3 function\$3) adj2 (block unit module engine subunit element subsystem))	EPO; JPO; DERWENT; IBM_TDB
9	L11	15	7 and 9	EPO; JPO; DERWENT; IBM_TDB
10	L6	287	4 and 5	USPAT; US-PGPUB
11	L14	89	13 and @pd<19920610	USPAT; US-PGPUB
12	L15	218	(sequencer) near10 instruction near20 ((composite comput\$5 process\$3 operation\$3 function\$3) adj2 (block unit module engine subunit element subsystem))	USPAT; US-PGPUB
13	L16	12	3 and 15 not 6	USPAT; US-PGPUB
14	L19	332725	(status condition) near10 (communicat\$3 transfer\$4 network rout\$3 bus connect\$3 interconnect\$3 path line)	USPAT; US-PGPUB
15	L20	4912	19 near20 ((composite comput\$5 process\$3 operation\$3 function\$3) adj2 (block unit module engine subunit element subsystem))	USPAT; US-PGPUB
16	L22	186252	(status condition) near10 (communicat\$3 transfer\$4 network rout\$3 bus connect\$3 interconnect\$3 path line)	EPO; JPO; DERWENT
17	L23	1707	22 near20 ((composite comput\$5 process\$3 operation\$3 function\$3) adj2 (block unit module engine subunit element subsystem))	EPO; JPO; DERWENT; IBM_TDB
18	L24	1	7 and 23 not 11	EPO; JPO; DERWENT; IBM_TDB
19	L21	224	1 and 20 not 6	USPAT; US-PGPUB

	Docum ent ID	U	Title	Current OR
1	US 20040 04966 4 A1	<input type="checkbox"/>	Methods and apparatus to support conditional execution in a VLIW-based array processor with subword execution	712/226
2	US 20040 03989 9 A1	<input checked="" type="checkbox"/>	Methods and apparatus to support conditional execution in a VLIW-based array processor with subword execution	712/226
3	US 20030 14967 1 A1	<input checked="" type="checkbox"/>	License information exchange system	705/59
4	US 20030 11508 3 A1	<input checked="" type="checkbox"/>	HTML-based clinical content	705/2
5	US 20030 10120 0 A1	<input checked="" type="checkbox"/>	Distributed file sharing system and a file access control method of efficiently searching for access rights	707/200
6	US 20030 07226 3 A1	<input checked="" type="checkbox"/>	Method and apparatus for monitoring and logging the operation of a distributed processing system	370/235
7	US 20030 07005 9 A1	<input checked="" type="checkbox"/>	System and method for performing efficient conditional vector operations for data parallel architectures	712/7
8	US 20030 06160 1 A1	<input checked="" type="checkbox"/>	Data processing apparatus and method, computer program, information storage medium, parallel operation apparatus, and data processing system	717/144
9	US 20030 04640 2 A1	<input checked="" type="checkbox"/>	Information processing apparatus and method, recording medium product, and program	709/228
10	US 20030 00717 8 A1	<input checked="" type="checkbox"/>	Information processing apparatus and control method therefor	358/1.1 5
11	US 20020 18856 2 A1	<input checked="" type="checkbox"/>	Billing system, and device constituting same	705/40
12	US 20020 17834 5 A1	<input checked="" type="checkbox"/>	Methods and apparatus to support conditional execution in a VLIW-based array processor with subword execution	712/24
13	US 20020 08784 7 A1	<input checked="" type="checkbox"/>	Method and apparatus for processing a predicated instruction using limited predicate slip	712/233
14	US 20020 08317 3 A1	<input checked="" type="checkbox"/>	Method and apparatus for optimizing selection of available contexts for packet processing in multi-stream packet processing	709/225
15	US 20020 05990 8 A1	<input checked="" type="checkbox"/>	Control system and method for operating an internal combustion engine	123/90. 11
16	US 20020 00745 0 A1	<input checked="" type="checkbox"/>	Line-oriented reorder buffer	712/23
17	US 20010 03115 0 A1	<input checked="" type="checkbox"/>	Image forming apparatus capable of processing images of plural documents	399/82

	Docum ent ID	U	Title	Current OR
18	US 20010 01694 7 A1	<input checked="" type="checkbox"/>	TV PLANNER FOR DSS	725/51
19	US 20010 01581 5 A1	<input checked="" type="checkbox"/>	IMAGE FORMING APPARATUS WHICH EXCELS IN REPRODUCIBILITY OF COLORS, FINE LINES AND GRADATIONS EVEN IN A COPY MADE FROM A COPIED IMAGE	358/1.9
20	US 66978 78 B1	<input checked="" type="checkbox"/>	Computer having a remote procedure call mechanism or an object request broker mechanism, and data transfer method for the same	719/316
21	US 66717 62 B1	<input checked="" type="checkbox"/>	System and method of saving and restoring registers in a data processing system	710/267
22	US 65671 76 B1	<input checked="" type="checkbox"/>	Information processing apparatus and control method therefor	358/1.1 4
23	US 65128 99 B2	<input checked="" type="checkbox"/>	Image forming apparatus capable of processing images of plural documents	399/82
24	US 64938 19 B1	<input checked="" type="checkbox"/>	Merging narrow register for resolution of data dependencies when updating a portion of a register in a microprocessor	712/210
25	US 64810 10 B2	<input checked="" type="checkbox"/>	TV planner for DSS	725/44
26	US 64532 77 B1	<input checked="" type="checkbox"/>	Virtual I/O emulator in a mainframe environment	703/24
27	US 64426 27 B1	<input checked="" type="checkbox"/>	Output FIFO data transfer control device	710/52
28	US 64351 47 B1	<input checked="" type="checkbox"/>	Control system and method for operating an internal combustion engine	123/90. 11
29	US 64306 46 B1	<input checked="" type="checkbox"/>	Method and apparatus for interfacing a processor with a bus	710/305
30	US 64012 19 B1	<input checked="" type="checkbox"/>	Failure analysis system, method for managing estimated logic status and information storage medium for programmed instruction of the method	714/26
31	US 63935 49 B1	<input checked="" type="checkbox"/>	Instruction alignment unit for routing variable byte-length instructions	712/204
32	US 63887 68 B2	<input checked="" type="checkbox"/>	Image forming apparatus which excels in reproducibility of colors, fine lines and gradations even in a copy made from a copied image	358/1.9
33	US 63816 89 B2	<input checked="" type="checkbox"/>	Line-oriented reorder buffer configured to selectively store a memory operation result in one of the plurality of reorder buffer storage locations corresponding to the executed instruction	712/215
34	US 63669 99 B1	<input checked="" type="checkbox"/>	Methods and apparatus to support conditional execution in a VLIW-based array processor with subword execution	712/24
35	US 63569 84 B1	<input checked="" type="checkbox"/>	Digital data processing system having a data bus and a control bus	711/147
36	US 63518 01 B1	<input checked="" type="checkbox"/>	Program counter update mechanism	712/205
37	US 63512 70 B1	<input checked="" type="checkbox"/>	Miniature video in the guide logo	345/717
38	US 63489 32 B1	<input checked="" type="checkbox"/>	Provide two different types of service in a menu	345/719
39	US 63395 92 B1	<input checked="" type="checkbox"/>	Apparatus and method of connecting computer network to telephone	370/352

	Docum ent ID	U	Title	Current OR
40	US 63112 25 B1	<input checked="" type="checkbox"/>	Method and apparatus for transferring data between process modules	719/310
41	US 63082 50 B1	<input checked="" type="checkbox"/>	Method and apparatus for processing a set of data values with plural processing units mask bits generated by other processing units	712/5
42	US 62984 35 B1	<input checked="" type="checkbox"/>	Methods and apparatus for exploiting virtual buffers to increase instruction parallelism in a pipelined processor	712/217
43	US 62984 17 B1	<input checked="" type="checkbox"/>	Pipelined cache memory deallocation and storeback	711/143
44	US 62694 36 B1	<input checked="" type="checkbox"/>	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
45	US 62370 82 B1	<input checked="" type="checkbox"/>	Reorder buffer configured to allocate storage for instruction results corresponding to predefined maximum number of concurrently receivable instructions independent of a number of instructions received	712/215
46	US 61957 44 B1	<input checked="" type="checkbox"/>	Unified multi-function operation scheduler for out-of-order execution in a superscalar processor	712/215
47	US 61890 89 B1	<input checked="" type="checkbox"/>	Apparatus and method for retiring instructions in excess of the number of accessible write ports	712/218
48	US 61890 68 B1	<input checked="" type="checkbox"/>	Superscalar microprocessor employing a data cache capable of performing store accesses in a single clock cycle	711/3
49	US 61855 65 B1	<input checked="" type="checkbox"/>	System and method for communication session disposition responsive to events in a telecommunications network and the internet	707/10
50	US 61450 49 A	<input checked="" type="checkbox"/>	Method and apparatus for providing fast switching between floating point and multimedia instructions using any combination of a first register file set and a second register file set	710/267
51	US 60981 67 A	<input checked="" type="checkbox"/>	Apparatus and method for fast unified interrupt recovery and branch recovery in processors supporting out-of-order execution	712/218
52	US 60946 89 A	<input checked="" type="checkbox"/>	System for coupling a host computer to an image scanner in which high level functions are migrated to the attached host computer	710/5
53	US 60818 54 A	<input checked="" type="checkbox"/>	System for providing fast transfers to input/output device by assuring commands from only one application program reside in FIFO	710/37
54	US 60578 35 A	<input checked="" type="checkbox"/>	Window management system with recording status display	345/759
55	US 60353 86 A	<input checked="" type="checkbox"/>	Program counter update mechanism	712/205
56	US 60264 82 A	<input checked="" type="checkbox"/>	Recorder buffer and a method for allocating a fixed amount of storage for instruction results independent of a number of concurrently dispatched instructions	712/215
57	US 60237 38 A	<input checked="" type="checkbox"/>	Method and apparatus for accelerating the transfer of graphical images	710/23
58	US 60147 34 A	<input checked="" type="checkbox"/>	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
59	US 60063 24 A	<input checked="" type="checkbox"/>	High performance superscalar alignment unit	712/204
60	US 59960 67 A	<input checked="" type="checkbox"/>	Range finding circuit for selecting a consecutive sequence of reorder buffer entries using circular carry lookahead	712/224
61	US 59875 61 A	<input checked="" type="checkbox"/>	Superscalar microprocessor employing a data cache capable of performing store accesses in a single clock cycle	711/3

	Docum ent ID	U	Title	Current OR
62	US 59833 42 A	<input checked="" type="checkbox"/>	Superscalar microprocessor employing a future file for storing results into multiportion registers	712/218
63	US 59789 07 A	<input checked="" type="checkbox"/>	Delayed update register for an array	712/239
64	US 59745 35 A	<input checked="" type="checkbox"/>	Method and system in data processing system of permitting concurrent processing of instructions of a particular type	712/215
65	US 59742 40 A	<input checked="" type="checkbox"/>	Method and system for buffering condition code data in a data processing system having out-of-order and speculative instruction execution	712/218
66	US 59737 12 A	<input checked="" type="checkbox"/>	Image recording apparatus	347/188
67	US 59702 35 A	<input checked="" type="checkbox"/>	Pre-decoded instruction cache and method therefor particularly suitable for variable byte-length instructions	712/213
68	US 59681 69 A	<input checked="" type="checkbox"/>	Superscalar microprocessor stack structure for judging validity of predicted subroutine return addresses	712/239
69	US 59639 73 A	<input checked="" type="checkbox"/>	Multiprocessor computer system incorporating method and apparatus for dynamically assigning ownership of changeable data	711/130
70	US 59616 34 A	<input checked="" type="checkbox"/>	Reorder buffer having a future file for storing speculative instruction execution results	712/218
71	US 59598 59 A	<input checked="" type="checkbox"/>	Plant monitoring/controlling apparatus	700/2
72	US 59516 74 A	<input checked="" type="checkbox"/>	Object-code compatible representation of very long instruction word programs	712/210
73	US 59502 27 A	<input checked="" type="checkbox"/>	CPU write-back cache coherency mechanism that transfers data from a cache memory to a main memory after access of the main memory by an alternative bus master	711/143
74	US 59464 68 A	<input checked="" type="checkbox"/>	Reorder buffer having an improved future file for storing speculative instruction execution results	712/218
75	US 59419 83 A	<input checked="" type="checkbox"/>	Out-of-order execution using encoded dependencies between instructions in queues to determine stall values that control issuance of instructions from the queues	712/214
76	US 59352 39 A	<input checked="" type="checkbox"/>	Parallel mask decoder and method for generating said mask	712/224
77	US 59336 18 A	<input checked="" type="checkbox"/>	Speculative register storage for storing speculative results corresponding to register updated by a plurality of concurrently recorded instruction	712/217
78	US 59266 44 A	<input checked="" type="checkbox"/>	Instruction formats/instruction encoding	712/22
79	US 59151 10 A	<input checked="" type="checkbox"/>	Branch misprediction recovery in a reorder buffer having a future file	712/239
80	US 59130 48 A	<input checked="" type="checkbox"/>	Dispatching instructions in a processor supporting out-of-order execution	712/215
81	US 59095 65 A	<input checked="" type="checkbox"/>	Microprocessor system which efficiently shares register data between a main processor and a coprocessor	712/200
82	US 59037 41 A	<input checked="" type="checkbox"/>	Method of allocating a fixed reorder buffer storage line for execution results regardless of a number of concurrently dispatched instructions	712/218
83	US 59037 40 A	<input checked="" type="checkbox"/>	Apparatus and method for retiring instructions in excess of the number of accessible write ports	712/217
84	US 59013 02 A	<input checked="" type="checkbox"/>	Superscalar microprocessor having symmetrical, fixed issue positions each configured to execute a particular subset of instructions	712/215

	Docum ent ID	U	Title	Current OR
85	US 58931 54 A	<input checked="" type="checkbox"/>	CPU write-back cache coherency mechanism that transeers data from a cache memory to a main memory before access of the main memory by an alternate bus master	711/143
86	US 58929 36 A	<input checked="" type="checkbox"/>	Speculative register file for storing speculative register states and removing dependencies between instructions utilizing the register	712/216
87	US 58896 69 A	<input checked="" type="checkbox"/>	Programmable controller allowing an external peripheral device to monitor an internal operation state of a CPU unit	700/17
88	US 58871 61 A	<input checked="" type="checkbox"/>	Issuing instructions in a processor supporting out-of-order execution	712/244
89	US 58871 52 A	<input checked="" type="checkbox"/>	Load/store unit with multiple oldest outstanding instruction pointers for completing store and load/store miss instructions	712/217
90	US 58840 59 A	<input checked="" type="checkbox"/>	Unified multi-function operation scheduler for out-of-order execution in a superscalar processor	712/215
91	US 58812 78 A	<input checked="" type="checkbox"/>	Return address prediction system which adjusts the contents of return stack storage to enable continued prediction after a mispredicted branch	712/242
92	US 58782 55 A	<input checked="" type="checkbox"/>	Update unit for providing a delayed update to a branch prediction array	712/240
93	US 58782 44 A	<input checked="" type="checkbox"/>	Reorder buffer configured to allocate storage capable of storing results corresponding to a maximum number of concurrently receivable instructions regardless of a number of instructions received	712/218
94	US 58753 24 A	<input checked="" type="checkbox"/>	Superscalar microprocessor which delays update of branch prediction information in response to branch misprediction until a subsequent idle clock	712/238
95	US 58753 15 A	<input checked="" type="checkbox"/>	Parallel and scalable instruction scanning unit	712/204
96	US 58729 51 A	<input checked="" type="checkbox"/>	Reorder buffer having a future file for storing speculative instruction execution results	712/218
97	US 58647 07 A	<input checked="" type="checkbox"/>	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
98	US 58601 10 A	<input checked="" type="checkbox"/>	Conference maintenance method for cache memories in multi-processor system triggered by a predetermined synchronization point and a predetermined condition	711/141
99	US 58601 04 A	<input checked="" type="checkbox"/>	Data cache which speculatively updates a predicted data cache storage location with store data and subsequently corrects mispredicted updates	711/137
100	US 58599 98 A	<input checked="" type="checkbox"/>	Hierarchical microcode implementation of floating point instructions for a microprocessor	712/222
101	US 58599 91 A	<input checked="" type="checkbox"/>	Parallel and scalable method for identifying valid instructions and a superscalar microprocessor including an instruction scanning unit employing the method	712/204
102	US 58570 89 A	<input checked="" type="checkbox"/>	Floating point stack and exchange instruction	712/222
103	US 58505 21 A	<input checked="" type="checkbox"/>	Apparatus and method for interprocessor communication	709/208
104	US 58484 33 A	<input checked="" type="checkbox"/>	Way prediction unit and a method for operating the same	711/137
105	US 58322 97 A	<input checked="" type="checkbox"/>	Superscalar microprocessor load/store unit employing a unified buffer and separate pointers for load and store operations	710/5
106	US 58322 49 A	<input checked="" type="checkbox"/>	High performance superscalar alignment unit	712/204

	Docum ent ID	U	Title	Current OR
107	US 58288 73 A	<input checked="" type="checkbox"/>	Assembly queue for a floating point unit	712/222
108	US 58260 71 A	<input checked="" type="checkbox"/>	Parallel mask decoder and method for generating said mask	712/224
109	US 58260 53 A	<input checked="" type="checkbox"/>	Speculative instruction queue and method therefor particularly suitable for variable byte-length instructions	712/210
110	US 58225 59 A	<input checked="" type="checkbox"/>	Apparatus and method for aligning variable byte-length instructions to a plurality of issue positions	712/214
111	US 58225 58 A	<input checked="" type="checkbox"/>	Method and apparatus for predecoding variable byte-length instructions within a superscalar microprocessor	712/213
112	US 58190 59 A	<input checked="" type="checkbox"/>	Predecode unit adapted for variable byte-length instruction set processors and method of operating the same	712/213
113	US 58190 57 A	<input checked="" type="checkbox"/>	Superscalar microprocessor including an instruction alignment unit with limited dispatch to decode units	712/204
114	US 58161 91 A	<input checked="" type="checkbox"/>	Stall manager system, module and feeding device for management of mealtimes and food distribution in animal stalls	119/57. 92
115	US 58157 23 A	<input checked="" type="checkbox"/>	Picket autonomy on a SIMD machine	712/20
116	US 57991 62 A	<input checked="" type="checkbox"/>	Program counter update mechanism	712/205
117	US 57907 84 A	<input checked="" type="checkbox"/>	Network for time synchronizing a digital information processing system with received digital information	370/520
118	US 57870 02 A	<input checked="" type="checkbox"/>	Control system for production facilities	700/115
119	US 57817 89 A	<input checked="" type="checkbox"/>	Superscaler microprocessor employing a parallel mask decoder	712/23
120	US 57686 10 A	<input checked="" type="checkbox"/>	Lookahead register value generator and a superscalar microprocessor employing same	712/23
121	US 57652 21 A	<input checked="" type="checkbox"/>	Method and system of addressing which minimize memory utilized to store logical addresses by storing high order bits within a register	711/220
122	US 57649 46 A	<input checked="" type="checkbox"/>	Superscalar microprocessor employing a way prediction unit to predict the way of an instruction fetch address and to concurrently provide a branch prediction address corresponding to the fetch address	712/239
123	US 57520 69 A	<input checked="" type="checkbox"/>	Superscalar microprocessor employing away prediction structure	712/23
124	US 57520 13 A	<input checked="" type="checkbox"/>	Method and apparatus for providing precise fault tracing in a superscalar microprocessor	712/227
125	US 56969 55 A	<input checked="" type="checkbox"/>	Floating point stack and exchange instruction	712/222
126	US 56946 03 A	<input checked="" type="checkbox"/>	Computer memory product with preemptive multithreading software	718/107
127	US 56896 93 A	<input checked="" type="checkbox"/>	Range finding circuit for selecting a consecutive sequence of reorder buffer entries using circular carry lookahead	712/224
128	US 56896 72 A	<input checked="" type="checkbox"/>	Pre-decoded instruction cache and method therefor particularly suitable for variable byte-length instructions	712/213

	Docum ent ID	U	Title	Current OR
129	US 56780 25 A	<input checked="" type="checkbox"/>	Cache coherency maintenance of non-cache supporting buses	711/135
130	US 56734 18 A	<input checked="" type="checkbox"/>	Method and apparatus for emulating the operations of an emulated system terminal driver on a host system	703/23
131	US 56641 99 A	<input checked="" type="checkbox"/>	Microcomputer free from control of central processing unit (CPU) for receiving and writing instructions into memory independent of and during execution of CPU	710/261
132	US 56551 15 A	<input checked="" type="checkbox"/>	Processor structure and method for watchpoint of plural simultaneous unresolved branch evaluation	712/239
133	US 56257 88 A	<input checked="" type="checkbox"/>	Microprocessor with novel instruction for signaling event occurrence and for providing event handling information in response thereto	712/214
134	US 56254 15 A	<input checked="" type="checkbox"/>	Apparatus and method for automatic focusing in a camera system	348/350
135	US 56175 74 A	<input checked="" type="checkbox"/>	Devices, systems and methods for conditional instructions	712/200
136	US 55599 75 A	<input checked="" type="checkbox"/>	Program counter update mechanism	712/230
137	US 55443 42 A	<input checked="" type="checkbox"/>	System and method for prefetching information in a processing system	711/119
138	US 55395 90 A	<input checked="" type="checkbox"/>	Floppy disk controller allowed to detect status change of floppy disk driver in standby mode	360/69
139	US 55376 02 A	<input checked="" type="checkbox"/>	Process system for controlling bus system to communicate data between resource and processor	712/38
140	US 55308 88 A	<input checked="" type="checkbox"/>	Process and apparatus for controlling a programmable controller with efficient identification of operation completion	710/5
141	US 55176 28 A	<input checked="" type="checkbox"/>	Computer with instructions that use an address field to select among multiple condition code registers	712/234
142	US 54816 85 A	<input checked="" type="checkbox"/>	RISC microprocessor architecture implementing fast trap and exception state	712/244
143	US 54816 78 A	<input checked="" type="checkbox"/>	Data processor including selection mechanism for coupling internal and external request signals to interrupt and DMA controllers	710/22
144	US 54758 52 A	<input checked="" type="checkbox"/>	Microprocessor implementing single-step or sequential microcode execution while in test mode	714/34
145	US 54487 05 A	<input checked="" type="checkbox"/>	RISC microprocessor architecture implementing fast trap and exception state	712/244
146	US 54370 48 A	<input checked="" type="checkbox"/>	Programmable controller acting as a master station and having automatic control of interlock process by using an operation complete address flag	709/208
147	US 54287 54 A	<input checked="" type="checkbox"/>	Computer system with clock shared between processors executing separate instruction streams	712/220
148	US 54189 73 A	<input checked="" type="checkbox"/>	Digital computer system with cache controller coordinating both vector and scalar operations	712/3
149	US 53676 92 A	<input checked="" type="checkbox"/>	Parallel computer system including efficient arrangement for performing communications among processing node to effect an array transposition operation	712/22
150	US 53296 30 A	<input checked="" type="checkbox"/>	System and method using double-buffer preview mode	711/173
151	US 53216 03 A	<input checked="" type="checkbox"/>	Programming apparatus for an industrial controller using two-dimensional graphic behavior profiles	700/17

	Docum ent ID	U	Title	Current OR
152	US 53094 44 A	<input checked="" type="checkbox"/>	Integrated circuit including a test cell for efficiently testing the accuracy of communication signals between a standard cell and an application cell	714/710
153	US 52915 81 A	<input checked="" type="checkbox"/>	Apparatus and method for synchronization of access to main memory signal groups in a multiprocessor data processing system	711/152
154	US 52860 37 A	<input checked="" type="checkbox"/>	Electronic hand held logic game	463/9
155	US 52768 02 A	<input checked="" type="checkbox"/>	Printer control system	385/115
156	US 52513 06 A	<input checked="" type="checkbox"/>	Apparatus for controlling execution of a program in a computing device	712/217
157	US 52261 70 A	<input checked="" type="checkbox"/>	Interface between processor and special instruction processor in digital data processing system	712/34
158	US 52261 49 A	<input checked="" type="checkbox"/>	Self-testing microprocessor with microinstruction substitution	714/25
159	US 52108 64 A	<input checked="" type="checkbox"/>	Pipelined microprocessor with instruction execution control unit which receives instructions from separate path in test mode for testing instruction execution pipeline	714/37
160	US 52010 52 A	<input checked="" type="checkbox"/>	System for transferring first and second ring information from program status word register and store buffer	710/260
161	US 51858 68 A	<input checked="" type="checkbox"/>	Apparatus having hierarchically arranged decoders concurrently decoding instructions and shifting instructions not ready for execution to vacant decoders higher in the hierarchy	712/217
162	US 51596 74 A	<input checked="" type="checkbox"/>	Method for supplying microcommands to multiple independent functional units having a next microcommand available during execution of a current microcommand	712/207
163	US 51270 91 A	<input checked="" type="checkbox"/>	System for reducing delay in instruction execution by executing branch instructions in separate processor while dispatching subsequent instructions to primary processor	712/238
164	US 51194 83 A	<input checked="" type="checkbox"/>	Application of state silos for recovery from memory management exceptions	714/15
165	US 51093 29 A	<input checked="" type="checkbox"/>	Multiprocessing method and arrangement	710/261
166	US 50937 75 A	<input checked="" type="checkbox"/>	Microcode control system for digital data processing system	712/212
167	US 50832 67 A	<input checked="" type="checkbox"/>	Horizontal computer having register multiconnect for execution of an instruction loop with recurrence	712/241
168	US 50420 00 A	<input checked="" type="checkbox"/>	Integral transform method	708/404
169	US 50382 77 A	<input checked="" type="checkbox"/>	Adjustable buffer for data communications in a data processing system	710/56
170	US 50364 76 A	<input checked="" type="checkbox"/>	Printer control system	358/1.1 8
171	US 50034 66 A	<input checked="" type="checkbox"/>	Multiprocessing method and arrangement	714/41
172	US 49339 41 A	<input checked="" type="checkbox"/>	Apparatus and method for testing the operation of a central processing unit of a data processing system	714/31
173	US 48721 06 A	<input checked="" type="checkbox"/>	Industrial process control system with back-up data processors to take over from failed primary data processors	714/13

	Docum ent ID	U	Title	Current OR
174	US 48602 44 A	<input checked="" type="checkbox"/>	Buffer system for input/output portion of digital data processing system	711/219
175	US 48315 20 A	<input checked="" type="checkbox"/>	Bus interface circuit for digital data processor	710/305
176	US 47424 51 A	<input checked="" type="checkbox"/>	Instruction prefetch system for conditional branch instruction for central processor unit	712/235
177	US 47408 93 A	<input checked="" type="checkbox"/>	Method for reducing the time for switching between programs	712/222
178	US 47187 59 A	<input checked="" type="checkbox"/>	Apparatus for the alignment and balance of the wheels of a motor vehicle	356/139 .09
179	US 47003 30 A	<input checked="" type="checkbox"/>	Memory for a digital data processing system including circuit for controlling refresh operations during power-up and power-down conditions	365/222
180	US 46047 50 A	<input checked="" type="checkbox"/>	Pipeline error correction	714/764
181	US 45832 22 A	<input checked="" type="checkbox"/>	Method and apparatus for self-testing of floating point accelerator processors	714/40
182	US 45532 01 A	<input checked="" type="checkbox"/>	Decoupling apparatus for verification of a processor independent from an associated data processing system	714/46
183	US 45272 47 A	<input checked="" type="checkbox"/>	Environmental control system	700/278
184	US 45272 37 A	<input checked="" type="checkbox"/>	Data processing system	709/253
185	US 45190 27 A	<input checked="" type="checkbox"/>	Industrial control, communications and information system	700/80
186	US 45161 99 A	<input checked="" type="checkbox"/>	Data processing system	710/20
187	US 44882 58 A	<input checked="" type="checkbox"/>	Programmable controller with control program comments	700/18
188	US 44868 49 A	<input checked="" type="checkbox"/>	Computer for calculating compound interest	708/134
189	US 44133 19 A	<input checked="" type="checkbox"/>	Programmable controller for executing block transfer with remote I/O interface racks	710/30
190	US 43947 25 A	<input checked="" type="checkbox"/>	Apparatus and method for transferring information units between processes in a multiprocessing system	718/106
191	US 43785 88 A	<input checked="" type="checkbox"/>	Buffer control for a data path system	710/57
192	US 43744 09 A	<input checked="" type="checkbox"/>	Method of and system using P and V instructions on semaphores for transferring data among processes in a multiprocessing system	718/106
193	US 43542 25 A	<input checked="" type="checkbox"/>	Intelligent main store for data processing systems	711/5
194	US 43251 19 A	<input checked="" type="checkbox"/>	Process and apparatus employing microprogrammed control commands for transferring information between a control processor and communications channels	710/5
195	US 43228 46 A	<input checked="" type="checkbox"/>	Self-evaluation system for determining the operational integrity of a data processing system	714/46
196	US 43204 51 A	<input checked="" type="checkbox"/>	Extended semaphore architecture	718/106

	Document ID	U	Title	Current OR
197	US 43181 82 A	<input checked="" type="checkbox"/>	Deadlock detection and prevention mechanism for a computer system	718/105
198	US 43162 45 A	<input checked="" type="checkbox"/>	Apparatus and method for semaphore initialization in a multiprocessing computer system for process synchronization	718/106
199	US 43131 61 A	<input checked="" type="checkbox"/>	Shared storage for multiple processor systems	711/151
200	US 43089 59 A	<input type="checkbox"/>	Roll sorting apparatus	209/563